A NEW REDUCED SWITCH COUNT PULSE WIDTH MODULATED MULTILEVEL INVERTER

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Abstract: The paper develops a new topology for a single phase cascaded H- Bridge multilevel inverter (CHB MLI) with a focus to reduce the number of power switching devices in the path for the flow of current. The philosophy combines an array of series connected voltage sources on either side of an H- bridge inverter to derive the new configuration for the MLI. It allows a Multicarrier Pulse Width Modulation (MCPWM) approach to the process of generating the pulses for synthesizing the PWM output voltage. The use of a smaller number of switches to reach the output voltage show cases the ability of the modular architecture to expand the scope of the CHBMLI. The architecture of a Field Programmable Gate Array (FPGA) fosters to realize its implementation and validate the simulated results over a range of modulation indices. The performance draws a new directive in the choice of a particular topology for the MLI to suit applications in the real world.

Key Words: ***Multi Level Inverters, Multicarrier Pulse Width Modulation, Field Programmable Gate Array***

1. Introduction

The Multilevel inverter (MLI) technology continues to emerge as a significant alternative to the traditional mechanisms in the area of high-power medium-voltage energy control**.** The theory of multilevel inversion owes to be a power conversion strategy where in the output voltage obtained in steps resembles the shape closer to that of a sine wave [1, 2]. The MLIs claim an inimitable

range of use in medium voltage drive applications to ascertain its place over traditional inverters [3-5].

The MLI offers the most phenomenal solution for high power applications particularly in medium and high voltage levels. The operation revolves around the synthesis of a voltage waveform from several isolated dc voltage levels or split capacitors through clamping diodes and flying capacitors [6]. It ensembles the proper arrangement of power electronic switches and dc voltage sources to reach the specified number of levels in the output voltage. The increase in the number of levels accounts for a corresponding increase in the number of steps to enable the voltage waveform approach the shape of the sine wave more accurately.

A host of efforts have been in vogue to increase the number of voltage levels with reduced number of switching devices. The dc–ac conversion facility inherits a number of advantages over the conventional two-level inverters that include a capability to operate at higher voltages using traditional semiconductors, reduced common mode voltages, reduced dv/dt stresses, staircase waveform with better harmonic profile, smaller filter requirements, flexibility to operate on low- and high switching frequencies besides a possibility for fault-tolerant operation [7, 8].

A new multilevel inverter structure based on multilevel dc-link (MLDCL) concept has been espoused off using half bridge cells of cascaded cells, diode clamped phase leg and flying capacitor phase leg. It has been able to provide a dc voltage with a staircase shape approximating the rectified shape of a commanded sinusoidal wave with or without pulse width modulation to the H- Bridge which in turn alternates the polarity to produce an ac voltage [9, 10]. The main drawback of these topologies has been the utilization of full bridge inverter that operates at high output voltage and results inflexible design.

A new single-phase MLI topology has been proposed in [11] with the number of voltage levels increased through a split-wound coupled inductor within each inverter leg. The main advantage of this topology has been the facility to provide a low value of high-frequency current ripple in

the load circuit and reduced shoot-through fault against dc-rails. The split wound coupled inductor design has been a tedious process and cannot be extended for higher number of levels.

A new symmetrical cascaded MLI has been developed in [12] where the cascade connection of sub-cells achieved using two dc sources and four switches through an H-bridge inverter. The topology has not been flexible in generating all the levels and this approach needs basic units which have been connected in series and utilize more devices in the conduction path.

An isolated cascaded MLI, employing low-frequency three-phase transformers and a single dc input power source has been suggested to avail the use of lower number of power devices. The higher implementation cost has been related to the fact that the number of low-frequency transformers increases with simultaneous increase in the number of voltage levels [13–15].

A new hybrid topology has been enlivened in [16] with the twin objective of increasing the level number of the output waveform and decreasing the lower order harmonics thereby minimizing harmonic distortion. However the modulator design has been found to be cumbersome for higher voltage applications. A high frequency link based multilevel inverter that utilizes single dc source has been brought out to support the whole multilevel inverter unit drive with an inherent regulation of voltages supplied among the H- Bridges. The control of the output voltage across the different levels with the variable voltage characteristics has been the added merit to this topology and on the other hand, the transformer core design and implementation cost limits the inverter application [17].

A new topology with voltage sources arranged in series/parallel [18] or switched in cross connected fashion [19-21] has been laid down to reduce the number of devices while increasing the output voltage level. The structure has been generalized for any number of levels, extended to three phase applications and optimized with various constraints for a given number of voltage levels. The hybrid topologies have been experiencing loss of modularity and produce problems with switching frequency and restrictions on modulation and control method.

A new topology has been developed using series connection of half bridge cells inverters in [22] and makes use of phase disposition pulse width modulation to generate the gating signals for the power switches. The major drawback of this topology has been the increased requirement in the number of diodes while increasing the voltage levels. A new cascaded nine level MLI has been proposed [23] with the capacitor voltages clamped through bidirectional IGBT switches and an H-Bridge inverter. The cells of the transistor clamped MLI have been cascaded to increase the number of levels with reduced blocking voltages.

A new single phase cascaded MLI has been configured [24] with the voltage sources arranged in X-shape. It has been operated in symmetric mode with equal voltage source magnitudes and with different voltage source magnitudes to realize the asymmetric mode. While both the topologies have been endowed with the advantage of reduced power components compared to CHB and other asymmetric topologies, the symmetric topology claims a reduced blocking voltage and the asymmetric topology, a total blocking voltages equal to that of CHBMLI.

An innovative cross switched topology for MLI has been developed with reduced number of power components and without using high voltage switches compared to conventional topologies [25]. A new single phase semi cascaded MLI has been articulated with reduced number of switches using series connected sub multilevel inverter blocks [26]. It has been constituted from the connection of several half bridge cell units in an appropriate scheme with the help of six power switches.

A novel cascaded MLI has been framed using a module or cell and an H-Bridge inverter [27]. The modules have been connected in series depending on the number of levels and then applied across H- Bridge inverter for polarity reversal. It has been tailored to reduce the number of switches and voltage sources with lesser peak inverse voltage compared to the conventional topologies.

A novel cascaded MLI has been constituted of a single dc source and a module for level generation part and an H-Bridge inverter for polarity reversal [28]. The module has been basically comprised of three voltage sources and four semiconductor switches to allow reduction of power losses.

A novel transformer based cascaded MLI with a single dc source has been presented operated in both symmetric and asymmetric conditions. The benefits have been derived from the advantages of the use of a reduced number of power switches and reduced total peak inverse voltage of the switching components [29]. The main disadvantage of this approach has been the need to include a number of transformer windings that add up to overall volume and cost of the inverter.

Despite many attempts in recent years to introduce new topologies, still there exists a need to explore better topologies for MLIs in an effort to reduce the switch count and bring in improvements the quality of power transfer.

The main task therefore emphasizes to establish a new MLI based topology that requires a lower number of switches for arriving at the desired level of output from a structural amalgamation of an H bridge employed through PWM strategy. It orients to use a MCPWM mechanism for acquiring the pulses and envisage using a Field Programmable Gate Array (FPGA) based prototype to validate the simulation results.

2. Proposed Topology

The topology connects an array of voltage sources in additive nature by switching the appropriate devices and produces the required level of the output voltage. It seeks the same number of voltage sources to extract a higher number of voltage levels with a reduced switch count.

The Fig. 1a depicts the generalized topology along with isolated dc voltage sources (V_1-V_n) and (V_1'-V_n') integrated with an H- bridge inverter. The complementary switches (S_a-S_b-S_c) and (S_b'-S_a'- S_c') incite the polarity reversal in the H- bridge inverter. The switches (S_1-S_n) and (S_1'-S_n')

connects the dc voltage sources (V_1-V_n) and (V_1'-V_n') for synthesizing the positive and negative voltage levels in the load side. The proposed topology inherits the merit of using isolated series connected voltage sources either from a dc-link or a renewable energy sources like photovoltaic cells. An ac-dc converter along with an isolation transformer and a filter capacitor provides the series connected voltage sources.

The Tables 1 and 2 explain the operating modes for producing the positive/negative cycles of the output voltage across the load for seven and eleven level respectively. The switches (S_1, S_2, S_1') in the voltage generation side of the proposed topology depicted in Fig. 1b are switched only twice in each fundamental cycle. In the same way, the switches (S_a, S_a', S_b, S_b', S_c, S_c') in the H-bridge side are switched only once for polarity reversal in each fundamental cycle to synthesize the staircase waveform. It follows from Fig. 1c, Fig. 1d and table 1 that the switch pairs (S_1, S_a, S_c' S_a',) and (S_1, S_c, S_b, S_b') serve to pronounce $\pm V_1$ in the output voltage of seven level inverter. Similarly it follows from table 2 that the switch pairs (S_1, S_b, S_b', S_c) and (S_1', S_b, S_b', S_c') serve to pronounce V_1 and V_1' in the output voltage of eleven level inverter.

With equal magnitudes set for the input dc sources, the MLI operates in the symmetrical mode and the maximum output voltage and number of levels derives to be ($n \times V_{dc}$) and ($(2 \times n) +1$) respectively, where 'n' is the number of dc sources.

However for the proposed topology to function in the asymmetrical configuration, the magnitude of the voltage sources multiplies through a factor of 2 and the maximum output voltage and the number of levels becomes equal to ($(2 \times n)-1) \times V_{dc}$) and ($(4 \times n)-1$) respectively. The new MLI avails the use of 9 switching devices for 11 levels and 10 for 15 levels in relation to the conventional cascaded inverter with 12 devices for 11 levels and 16 for 15 levels with the same number of voltage sources.

The increase in the number of output voltage levels can also be brought about by changing the ratio of the voltages of the sources like in conventional cascaded H bridge (CHB) inverters.

Therefore higher the number of output levels, the difference between the required numbers of switching devices turns out to be larger between the two inverters. Hence both symmetrical and asymmetrical modes enjoy the need of lower number of switches in the conducting path than the cascaded MLI.

The Tables 3 and 4 compare the number of components with similar other architectures to establish the merits of the proposed CMLI. The number of components required between the symmetrical and asymmetrical mode in the proposed topology is tabulated in Table 5. The Fig. 2a depicts the variation of number of power components (IGBTs and diodes) required to produce an output voltage with a particular level with the same number of dc sources and the Fig. 2b shows that the number of power devices in the path for the current against the number of levels (m). The number of devices in the conduction path for 'm' level output voltage in a CHBMLI becomes equal to half the total number of devices. However the proposed MLI requires only a maximum of 5 devices in the conduction path irrespective of the number of levels because it involves 3 devices from H bridge unit and 2 devices to switch the voltage sources from the external arms on either side that remain connected to the H bridge.

The Fig.2c relates the efficiency of the proposed topology with that of the CHB MLI as a function of the modulation ratio (M), which is defined as the ratio of the output voltage peak to the sum of dc voltages. The efficiency relies on calculation of switching and conduction losses using the equations in [30] and the proposed topology enjoys a higher efficiency owing to the fact that there it involves lower number of switching devices in the path for the current at any instant of time.

However all the switches in the CHBMLI are switched for every cycle and as a result the switching loss will be much less for the proposed topology. Besides as the number of switches in conduction for each level of the output varies in the proposed topology the power loss deems to be asymmetric.

The MLI topology under study operates from a number of dc sources for synthesizing the output to a nearly sinusoidal waveform. The power output varies as a function of the modulation index, output voltage levels in addition to the load power factor. However the input dc sources deliver unequal power to result in rippled dc voltage levels and as a consequence the different dc sources face different lifetimes.

It becomes essential for the dc sources to share the load equally. For example a five level inverter with two voltage sources (V_1=V_1'=V_{dc}) allows the load to share equally if V_1 and V_1' remain engaged alternately in full cycles of the output waveform and balancing accomplished in two cycles. The MCPWM with pulse swapping method enables the five level output with equal load sharing.

The results of the five level inverter with V_1=V_1'=150V, R=150Ω and L=100mH seen in Fig. 3 depict the source currents to follow an alternating pattern as a result of swapping the two sources for the voltage level synthesis in alternate cycles. The effective charge/discharge of the two sources being identical serves to achieve charge balancing. The entries in Table 6 establish the equal contribution from the two input sources and indicate an effective load sharing.

It follows that for equal load sharing among the input dc sources, each source requires to contribute for synthesis of levels alternately. The three dc sources (V_1= V_2= V_1'= V_{dc}) enable the synthesis of levels $\pm V_{dc}$, $\pm 2V_{dc}$ and $\pm 3V_{dc}$ in combinations of (V_1 or V_2 or V_1'), (V_1+V_2 or V_1+V_1' or V_1'+V_2) and (V_1+V_2+V_1') respectively.

The approach becomes difficult to synthesize the voltage levels $\pm V_2$ and $\pm(V_1'+V_2)$ through any switching combination and consequently equal load sharing cannot be achieved. Therefore equal load sharing among all the input sources assumes a challenge in the event of the number of input dc sources being more than three.

However the proposed topology attains equal load sharing among some of the input sources, for example with three input sources, equal load sharing turns out to be a possibility among sources (V_1 and V_2) or among sources (V_1 and V_1').

3. Selection of devices

The blocking voltages being asymmetric across the switches in the proposed MLI however facilitate a lower number of switching devices in the current conduction path compared to the CHBMLI. The blocking voltage across the switches in the voltage generation part varies in accordance with the magnitude of the voltage source connected to the H- Bridge inverter. The blocking voltage across each switch is given by

$$S_i = S_i' = \sum_{j=1}^{i} V_{dc} \qquad i=1, 2, 3\ldots n \qquad (1)$$

The blocking voltage across the switches used for the reversal of the polarity is required to block the full dc-link voltages. The blocking voltage across each switch is given by

$$S_x = S_x' = \left(2 \times n \times V_{dc}\right) \qquad x=a, b, c \qquad (2)$$

4. Modulation Strategy

The attributes of pulse width modulation (PWM) govern the cohesive conduction of active devices in the MLI to assuage a desired output. The modulation methods relating to control the MLIs appear to be simply an extension of three level PWM. The modulations rely on the multiple carrier arrangements in the periphery of the PWM. The carriers can be arranged with vertical phase shifts like Phase Disposition (PD), Phase Opposite Disposition (POD), Alternative phase opposite Disposition (APOD), Carrier Polarity Variation (CPV) and horizontal Shifts namely Phase shifted Carrier (PSC) [31].

It espouses the nuances of a Multicarrier pulse width modulation (MCPWM) approach to control the switches in the proposed power module. The switching sequences seen in Tables 1 and 2 are implemented through the use of logical gates.

5. Simulation results

The procedure follows to test the proposed topology under symmetrical and asymmetrical configuration with following simulation parameters: voltage sources (V_1'= V_1= V_2) = 1:1:1 for symmetrical mode and (V_1'= V_1= V_2) = 1:2:2 to obtain 7 and 11 level single phase output of 212 volts at the fundamental frequency across a RL load of 150 Ω and 100mH on a MATLAB r2010a platform.

It engages the MCPWM method with a carrier frequency of 2 kHz as the firing strategy. The Figs. 4, 5 and 6 respectively display the output voltage, inductive load current, along with output voltage spectrum for 7 and 11 level inverters. The results serve to claim that the new structure carries the flexibility to extend to higher number of levels for any target output voltage.

6. Hardware results

The active elements IGBTs (FIO 5O-12BD and IRG4BC20SD) together with associated gate driver units form the prototype in Fig. 7 with similar simulation specifications and the theory of pulse generation methodology used in [23]. The procedure acquires the artifacts of a spartan architecture Xilinx Spartan 3E-500 FG 320 to realize the algorithm in the process of generating the pulses.

The Figs. 8, 9, 10 and 11, 12 portray the gating signals, output voltage along with harmonic spectrum and inductive load current waveform for seven and eleven level inverters respectively corresponding to a modulation index of 1 for an output of 210V are captured through Tektronix TPS 2024 scope respectively.

7. Conclusion

A new CMLI based topology has been fortified to facilitate the reduction in the switch count through the path for the flow of current to reach the different levels of output voltage. The theory has been conceived to increase the number of voltage levels through an architecture that combines an H-bridge inverter along with the requisite number of isolated dc sources on either side. The benefits have been unequivocally translated to enjoy a reduction in the use of a smaller

number of active devices. The simulation responses have been echoed to illustrate its viability and the experimental results laid to validate its credibility for use in the real world. The fact that the methodology has been cast to acquire any number of preferred levels will go a long in adding substance to this new topology.

8. References

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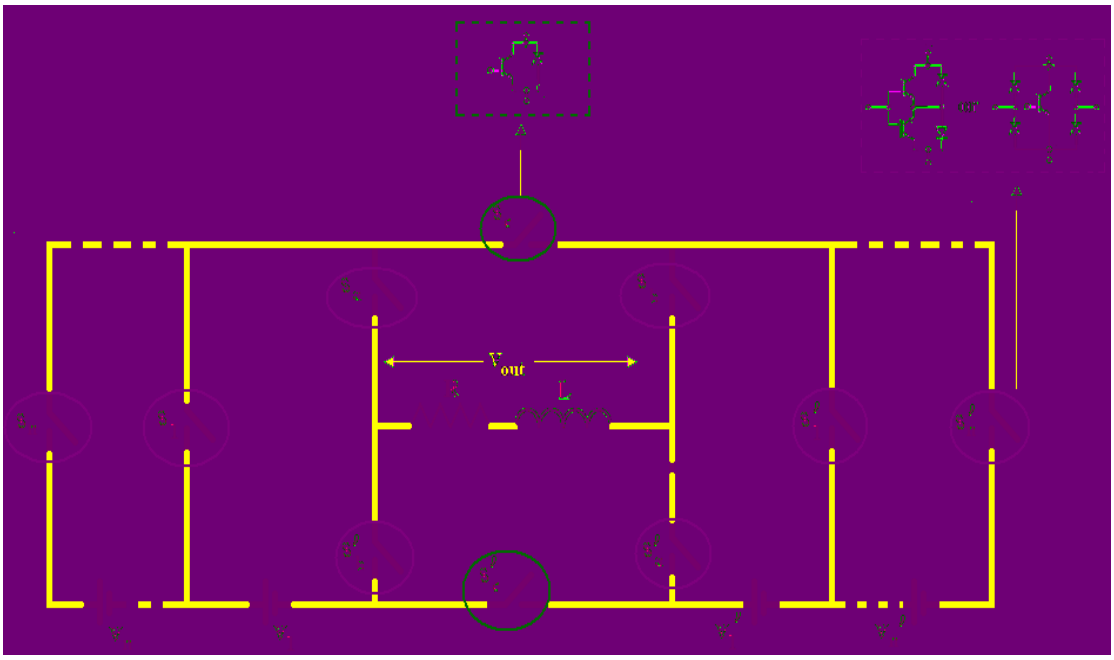
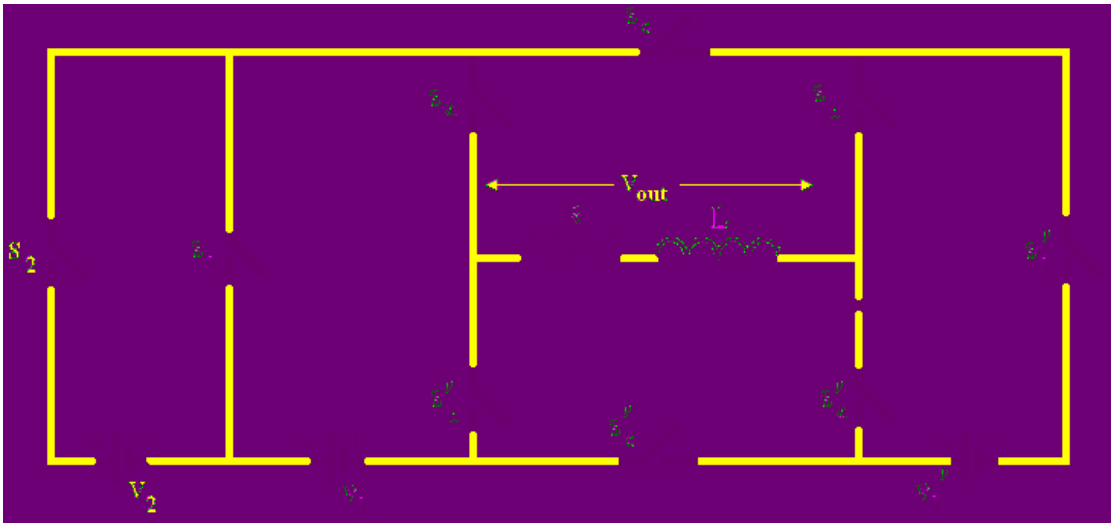


(a)



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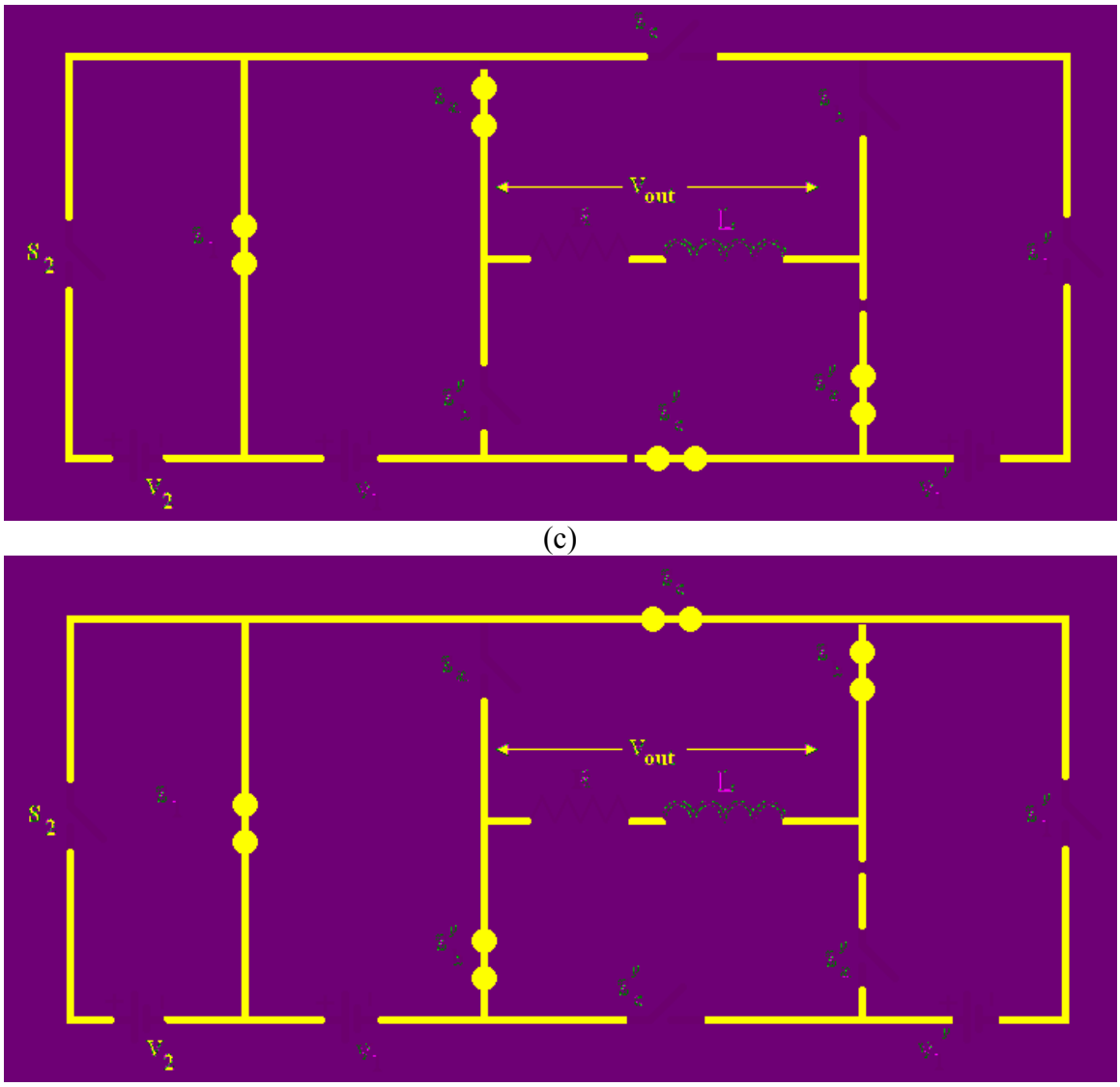
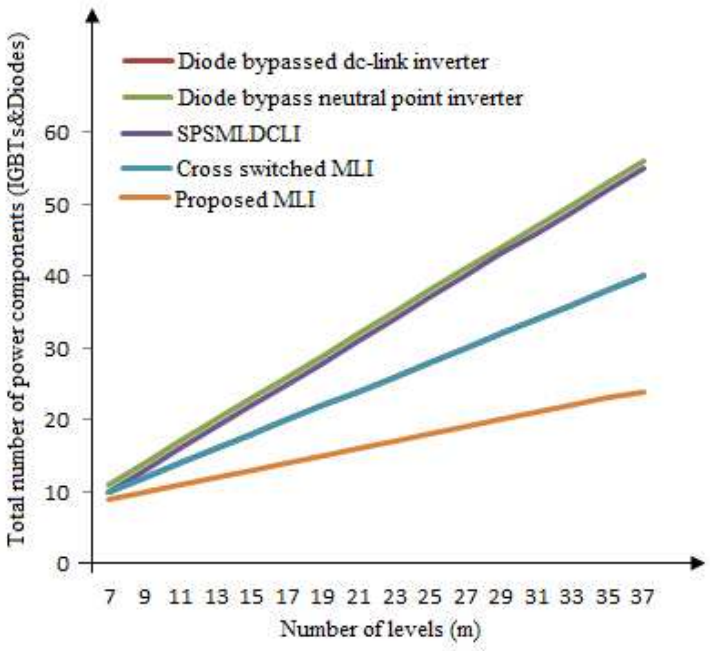


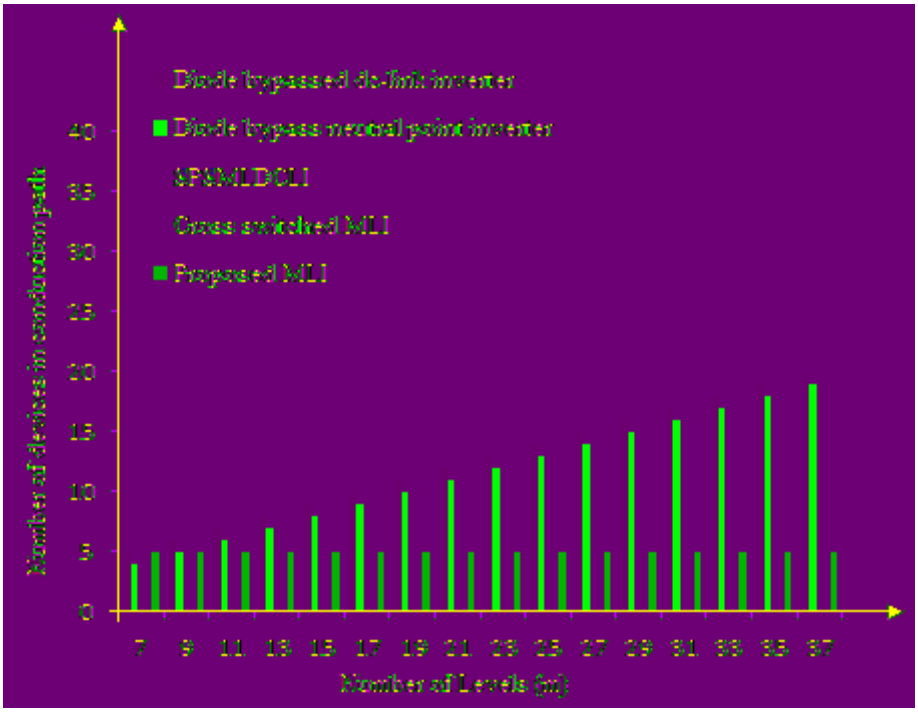
(c)

(d)

Fig. 1 (a) Generalized topology (b) Seven level inverter (c) Operating mode to extract voltage level $+V_1$ (d) Operating mode to extract voltage level $-V_1$



(a)



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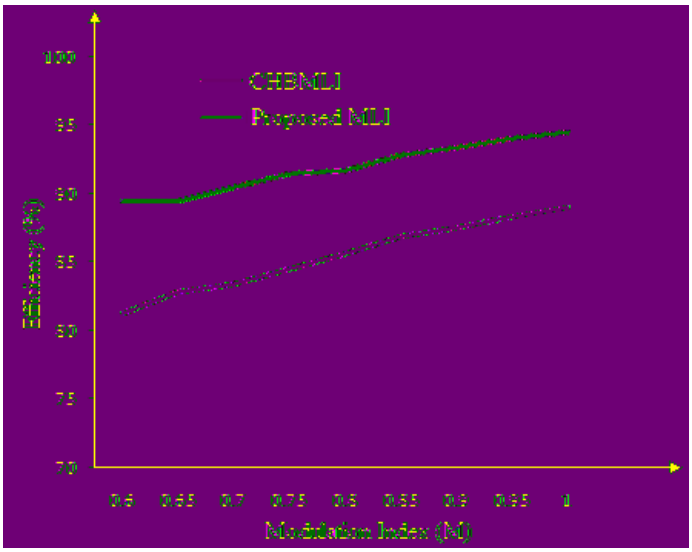


(c)

Fig. 2 (a) Variation of power components against number of levels **(b)** Variation of devices in conduction path against number of levels **(c)** Variation of Efficiency against Modulation Index

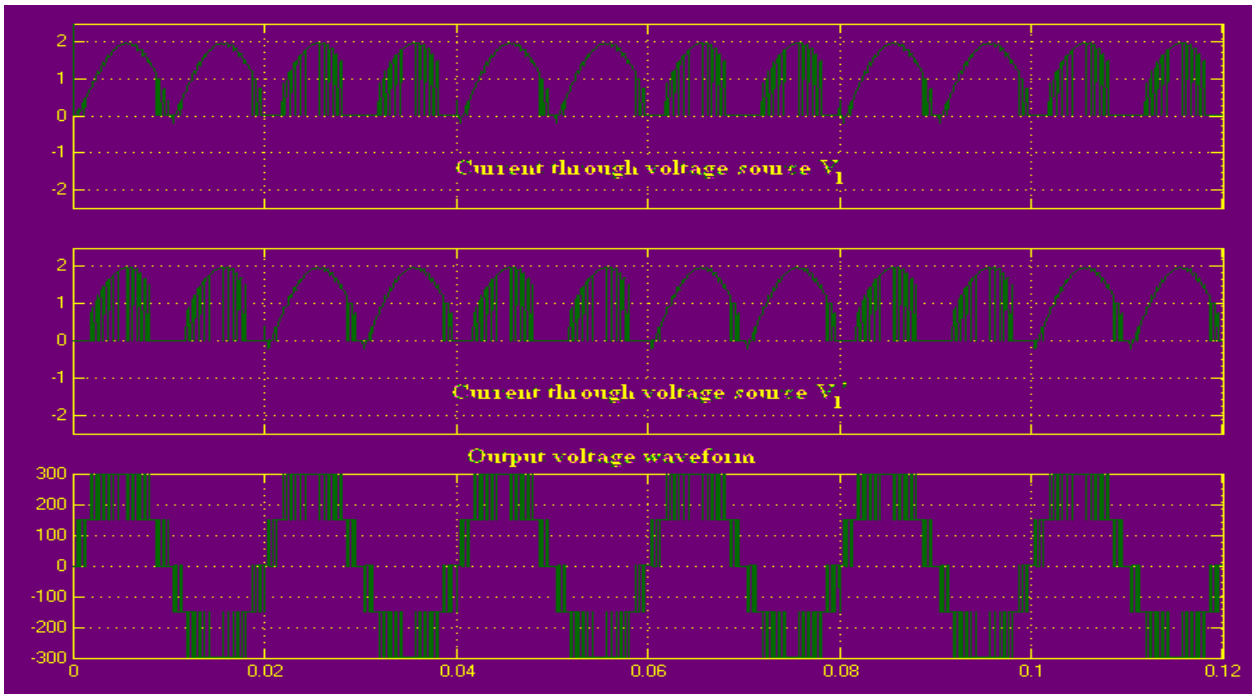
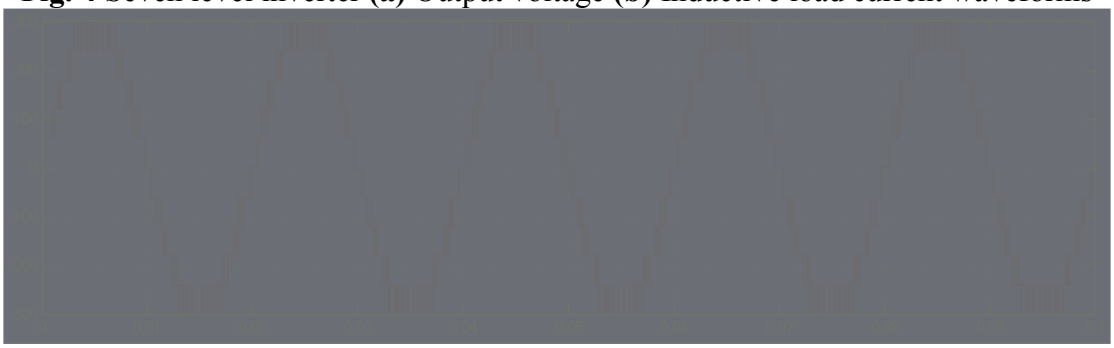


Fig. 3 Simulated results for five level inverter with power balancing algorithm

(a)

(b)

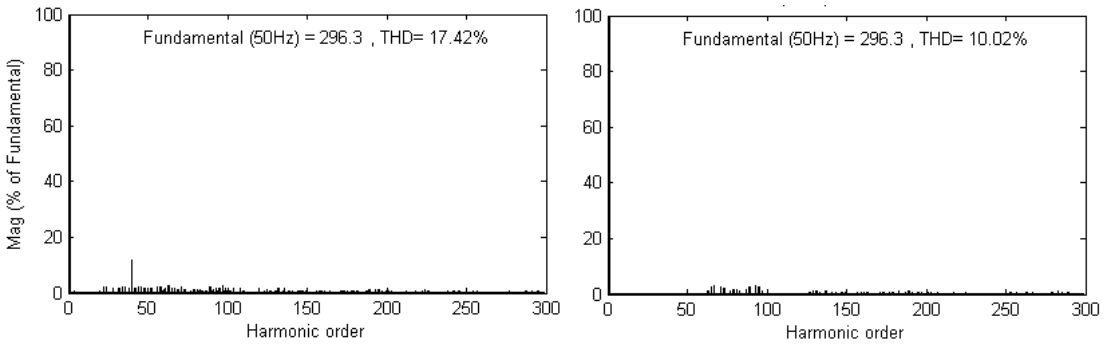
Fig. 4 Seven level inverter **(a)** Output voltage **(b)** Inductive load current waveforms



(a)

(b)

Fig. 5 (a) Output voltage waveform **(b)** Inductive load current waveform for eleven level inverter



(a) (b)

Fig. 6 Output voltage spectrum (a) Seven level (b) Eleven level

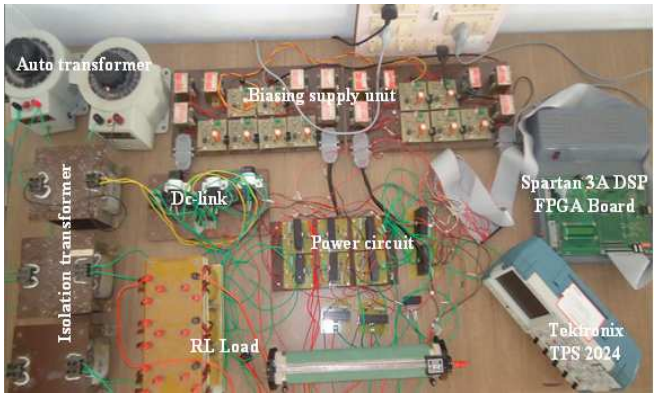


Fig. 7 Experimental setup

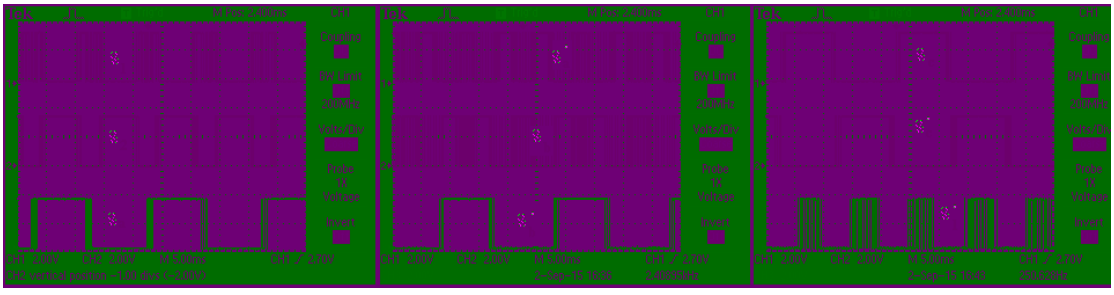


Fig. 8 Gating pulses for seven level inverter

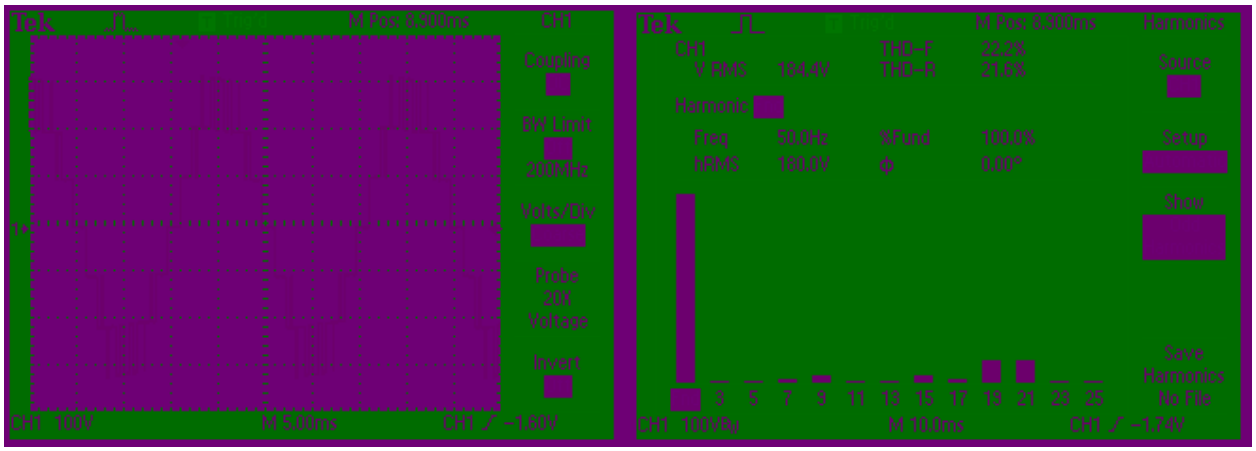


Fig. 9 Seven level inverter (a) Output voltage waveform (b) Harmonic spectrum

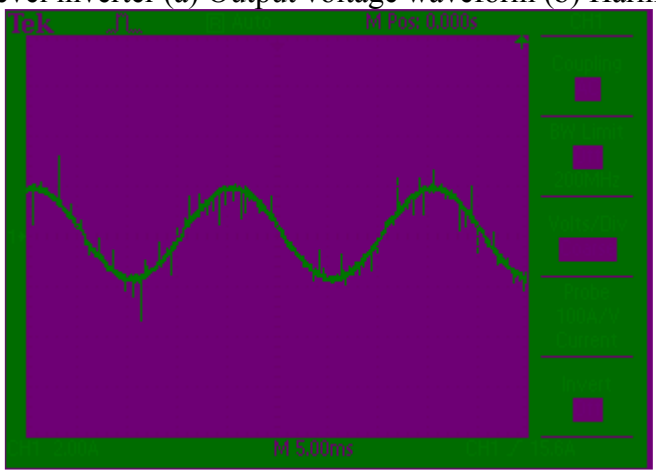


Fig. 10 Inductive load current waveform for seven level inverter

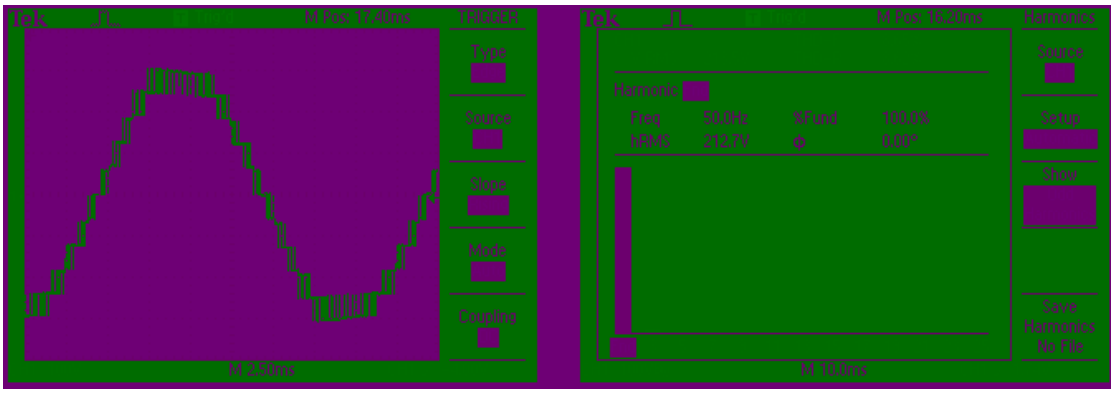


Fig. 11 Eleven level inverter (a) Output voltage waveform (b) Harmonic spectrum

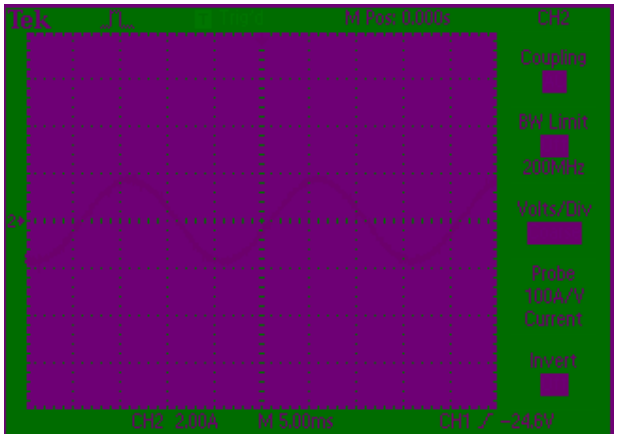


Fig. 12 Inductive load current waveform for eleven level inverter

Table1 Switching table for seven level inverter

Output voltage level	S_1	S_2	S_1'	S_a	S_a'	S_b	S_b'	S_c	S_c'
V_1	√			√	√				√
(V_1+V_2)		√		√	√				√
$(V_1+V_2+V_1')$		√	√	√		√			√
0				√		√		√	
$-V_1$	√					√	√	√	
$-(V_1+V_2)$		√				√	√	√	
$-(V_1+V_2+V_1')$		√	√		√		√	√	

Table 2 Switching table for eleven level inverter

Output voltage level	S_1	S_2	S_1'	S_a	S_a'	S_b	S_b'	S_c	S_c'
V_1'			√			√	√		√
V_1	√					√	√	√	
$(V_1+ V_1')$	√		√	√		√			√
(V_1+V_2)		√		√	√				√
$(V_1+V_2+V_1')$		√	√	√		√			√
0				√		√		√	
$-V_1'$			√	√	√			√	
$-V_1$	√					√	√	√	
$-(V_1+ V_1')$	√		√		√		√	√	
$-(V_1+V_2)$		√				√	√	√	
$-(V_1+V_2+V_1')$		√	√		√		√	√	

Table 3 Comparison between proposed and conventional topologies for 'm' level

Multilevel inverter structure	**Cascaded H-bridge**	**Diode clamped (1981)**	**Flying Capacitor**	**Multilevel dc-link inverter**			**Proposed**
				Cascaded half bridge	**Diode Clamped**	**Flying capacitor**	
Main switches	2(m-1)	2(m-1)	2(m-1)	(m-1)+4	(m-1)+4	(m-1)+4	(m+11)/2
Bypass diodes	-	-	-	-	-	-	-
Clamping diodes	-	2(m-3)	-	-	(m-3)	-	-
DC split capacitors	-	(m-1)/2	(m-1)/2	-	(m-1)/2	(m-1)/2	-
Clamping capacitors	-	-	(2m-6)/2	-	-	(2m-6)/4	-
DC sources	(m-1)/2	1	1	(m-1)/2	1	1	(m-1)/2

Table 4 Comparison between proposed and similar topologies for 'm' level

Multilevel inverter structure	Diode bypassed dc-link inverter	Diode bypass neutral point inverter	SPSMLDCLI	Cross switched MLI	Proposed
Main switches	(m+7)/2	(m+1)	(3m-1)/2	(m+3)	(m+11)/2
Bypass diodes	(m-1)/2	(m-1)/2	1	-	-
Clamping diodes	-	-	-	-	-
DC split capacitors	-	-	-	-	-
Clamping capacitors	-	-	-	-	-
No. of devices in the conduction path	(m+3)/2	(m+1)/2	(m-1)	(m+3)/2	5
DC sources	(m-1)/2	(m-1)/2	(m-1)/2	(m-1)/2	(m-1)/2

Table 5 Comparison of power components required for proposed inverters

Parameters	Symmetrical	Asymmetrical
No. of DC sources	n	n
No. of switches	n+6	n+6
No. of output levels	(2×n)+1	(4×n)-1
Maximum voltage	$n\times V_{dc}$	$((2\times n)-1)\times V_{dc}$
Standing voltages on all the switches (S_1-S_n) and (S_1'-S_n')	$n\times V_{dc}$	$((2\times n)-1)\times V_{dc}$
H- Bridge switches	$2\times n\times V_{dc}$	$((4\times n)-2)\times V_{dc}$

Table 6 Power delivered by the voltage sources

Output power	Input power	
	Power delivered by voltage source V_1	Power delivered by voltage source V_1'
304W	145W	145W